C. U. SHAH UNIVERSITY
Winter Examination-2020

Subject Name: Digital Circuits

Subject Code: 4TE03DCI1   **Branch: B.Tech (Electrical)**

Semester: 3   **Date: 10/03/2021**   **Time: 11:00 To 02:00**   **Marks: 70**

Instructions:
(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1   **Attempt the following questions:**   **(14)**

a) Which of these sets of logic gates are designated as universal gates?
a) NOR, NAND.
b) XOR, NOR, NAND.
c) OR, NOT, AND.
d) NOR, NAND, XNOR.

b) Which of the following is a digital device?
a) Regulator of a fan
b) Microphone
c) Resistance of a material
d) Light switch

c) If a Hexadecimal number needs to convert to binary. For each hexadecimal digit, there will be how many bits
a) 1
b) 2
c) 4
d) 8

d) Complement of NOR and OR gate is _____ and _____ respectively.
a) AND, NAND
b) NAND, AND
c) NOR, OR
d) None of above

e) When will be the output of an AND gate is LOW?
a) When any input is LOW
b) When any input is HIGH
c) When all inputs are HIGH
d) When all input is LOW

f) Total number of inputs in a half adder is _____
a) 2

b) 3
c) 4
d) 1

g) The difference between half adder and full adder is _____
a) Half adder has two inputs while full adder has four inputs
b) Half adder has one output while full adder has two outputs
c) Half adder has two inputs while full adder has three inputs
d) All of the Mentioned

h) In a number system, each position of a digit represents a specific power of the base.
a) True
b) False

i) What does the symbol D represent in a hexadecimal number system?
a) 8
b) 16
c) 13
d) 14

j) A bit in a computer terminology means either 0 or 1.
a) True
b) False

k) The binary equivalent of the octal number $(0010010100)_2$ is _____

l) Most significant bit of arithmetic addition is called
(a) overflow (b) carry (c) output (d) zero bit

m) Code conversion circuits mostly uses
(a)AND-OR gates (b)AND gates (c)OR gates (d)XOR gates

n) Two-bit subtraction is done by
(a) demux (b) mux (c) full subtract (d) half subtract

Attempt any four questions from Q-2 to Q-8

Q-2	**Attempt all questions**	**(14)**
(a)	Compare digital system with analog system.	**(07)**
(b)	Give statement and explain De' morgens Theorem.	**(07)**
Q-3	**Attempt all questions**	**(14)**
(a)	Design and Implement a Half Adder.	**(07)**
(b)	Draw the logic symbol and construct the truth table for all logic gates.	**(07)**
Q-4	**Attempt all questions**	**(14)**
(a)	Write definition of Flip-flop and explain J-K flip flop.	**(07)**
(b)	Design and Implement a 3-line to 8-line decoder.	**(07)**
Q-5	**Attempt all questions**	**(14)**
(a)	Explain full adder circuit with truth table.	**(07)**
(b)	With neat sketch explain the operation of R-S flip flop.	**(07)**
Q-6	**Attempt all questions**	**(14)**
(a)	Convert $(10101)_2$ to decimal.	**(07)**

Convert $(1001011)_2$ to decimal.
Convert $(105.15)_{10}$ to binary.

Write 1st Complement of 1000101.

(b) Convert $(4BAC)_{16}$ to binary. **(07)**
Convert $(2598.675)_{10}$ to hex.
Add to Numbers: 11011+10001.
Multiply $(1101)_2$ to by $(110)_2$.

Q-7 **Attempt all questions** **(14)**
(a) Design and Implement a 1-line to 8-line demultiplexer. **(07)**
(b) What are the applications of shift register? **(07)**

Q-8 **Attempt all questions** **(14)**
(a) Comparison of Counters and Registers. **(07)**
(b) With neat diagram explain the operation of 4- bit parallel- in Serial-out Shift **(07)**
register.